

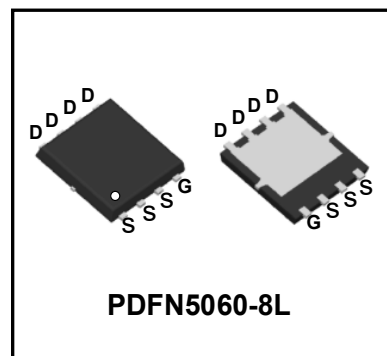
100V N-Channel Enhancement Mode Power MOSFET

Description

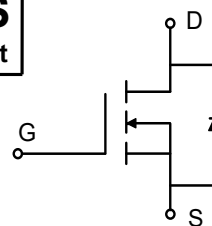
WMB080N10LG2 uses Wayon's 2nd generation power trench MOSFET technology that has been especially tailored to minimize the on-state resistance and yet maintain superior switching performance. This device is well suited for high efficiency fast switching applications.

Features

- $V_{DS} = 100V$, $I_D = 74A$
 $R_{DS(on)} < 8m\Omega$ @ $V_{GS} = 10V$
 $R_{DS(on)} < 11m\Omega$ @ $V_{GS} = 4.5V$
- Green Device Available
- 100% EAS Guaranteed
- Optimized for High Speed Smooth Switching



RoHS
compliant



Applications

- Power Management Switches
- DC/DC Converters
- Synchronous Rectification

Absolute Maximum Ratings ($T_A = 25^\circ C$, unless otherwise noted)

Parameter		Symbol	Value	Unit
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	± 20	V
Continuous Drain Current	$T_C = 25^\circ C$	I_D	74	A
	$T_C = 100^\circ C$		46.8	
Pulsed Drain Current ¹		I_{DM}	296	A
Single Pulse Avalanche Energy ²		EAS	88.2	mJ
Total Power Dissipation	$T_C = 25^\circ C$	P_D	84	W
Operating Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150	$^\circ C$

Thermal Characteristics

Parameter	Symbol	Value	Unit
Thermal Resistance from Junction-to-Ambient ³	$R_{\theta JA}$	50	$^\circ C/W$
Thermal Resistance from Junction-to-Case	$R_{\theta JC}$	1.48	$^\circ C/W$

Electrical Characteristics ($T_J = 25^{\circ}\text{C}$, unless otherwise noted)

Parameter		Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static Characteristics							
Drain-Source Breakdown Voltage		V _{(BR)DSS}	V _{GS} = 0V, I _D = 250μA	100	-	-	V
Gate-Body Leakage Current		I _{GSS}	V _{DS} = 0V, V _{GS} = ±20V	-	-	±100	nA
Zero Gate Voltage Drain Current	T _J =25°C	I _{DSS}	V _{DS} = 100V, V _{GS} = 0V	-	-	1	μA
	T _J =100°C			-	-	100	
Gate-Threshold Voltage		V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250μA	1.2	1.8	2.4	V
Drain-Source on-Resistance ⁴		R _{DS(on)}	V _{GS} = 10V, I _D = 20A	-	6.3	8	mΩ
			V _{GS} = 4.5V, I _D = 10A		7.8	11	
Forward Transconductance ⁴		g _{fs}	V _{DS} = 5V, I _D = 10A	-	56	-	S
Dynamic Characteristics ⁵							
Input Capacitance		C _{iss}	V _{DS} = 50V, V _{GS} =0V, f =1MHz	-	1920	-	pF
Output Capacitance		C _{oss}		-	359	-	
Reverse Transfer Capacitance		C _{rss}		-	9.7	-	
Gate Resistance		R _G	f =1MHz	-	1.0	-	Ω
Switching Characteristics ⁵							
Total Gate Charge		Q _g	V _{GS} = 10V, V _{DD} = 50V, I _D = 20A	-	30.8	-	nC
Gate-Source Charge		Q _{gs}		-	7.1	-	
Gate-Drain Charge		Q _{gd}		-	4.9	-	
Turn-on Delay Time		t _{d(on)}	V _{GS} =10V, V _{DD} = 50V, R _G = 3Ω, I _D = 20A	-	5.8	-	ns
Rise Time		t _r		-	3.2	-	
Turn-off Delay Time		t _{d(off)}		-	18.7	-	
Fall Time		t _f		-	4.2	-	
Body Diode Reverse Recovery Time		t _{rr}	I _F =20A, dI _F /dt=500A/μs	-	36	-	ns
Body Diode Reverse Recovery Charge		Q _{rr}		-	178	-	nC
Drain-Source Body Diode Characteristics							
Diode Forward Voltage ⁴		V _{SD}	I _S = 1A, V _{GS} = 0V	-	-	1.2	V
Continuous Source Current	T _C =25°C	I _S	-	-	-	74	A

Notes:

1. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)} = 150^{\circ}\text{C}$.
2. The EAS data shows Max. rating. The test condition is $V_{DD} = 25V, V_{GS} = 10V, L = 0.4mH, I_{AS} = 21A$.
3. The data tested by surface mounted on a 1 inch² FR-4 board with 20Z copper, The value in any given application depends on the user's specific board design.
4. The data tested by pulsed, pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$.
5. This value is guaranteed by design hence it is not included in the production test..

Typical Characteristics

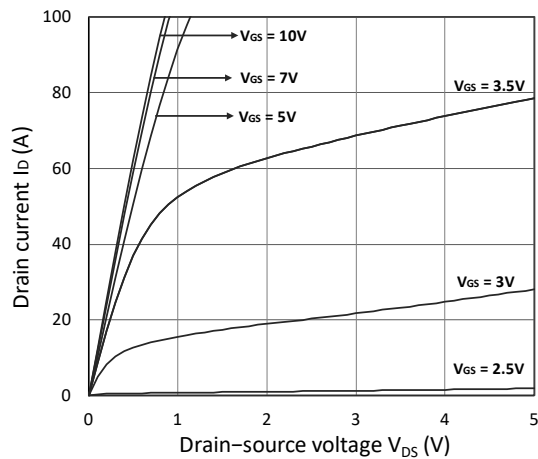


Figure 1. Output Characteristics

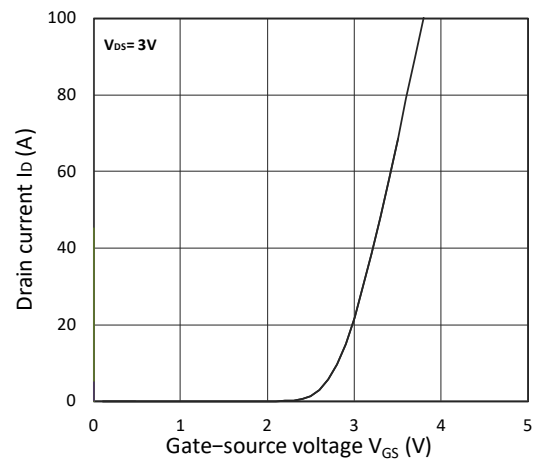


Figure 2. Transfer Characteristics

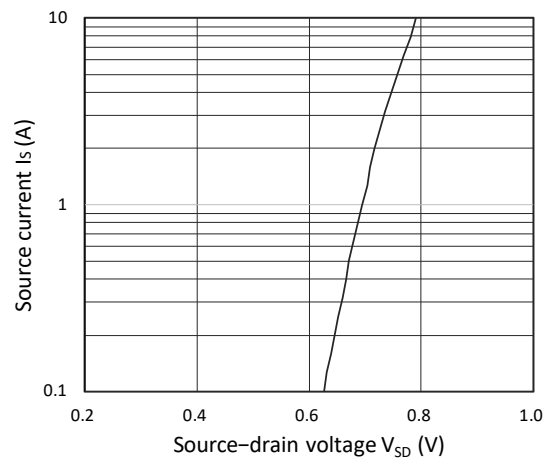
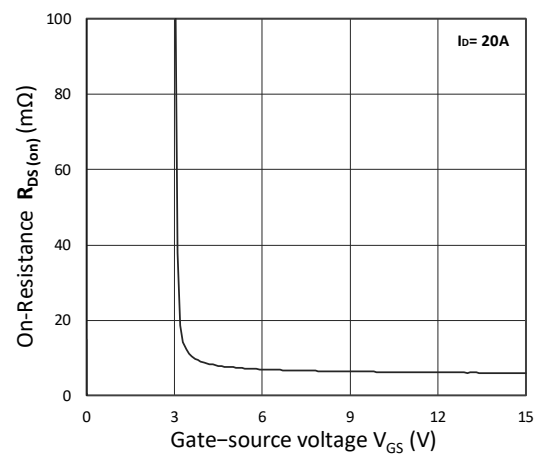
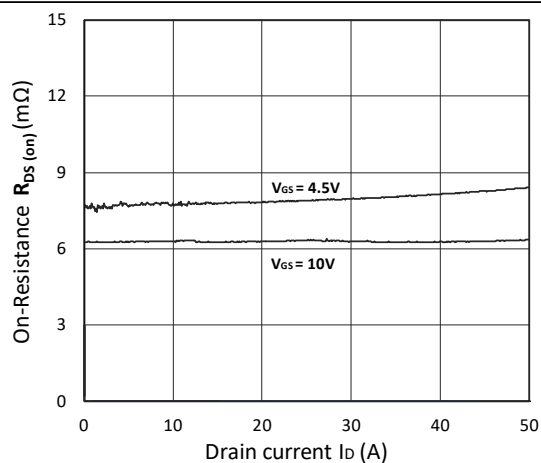
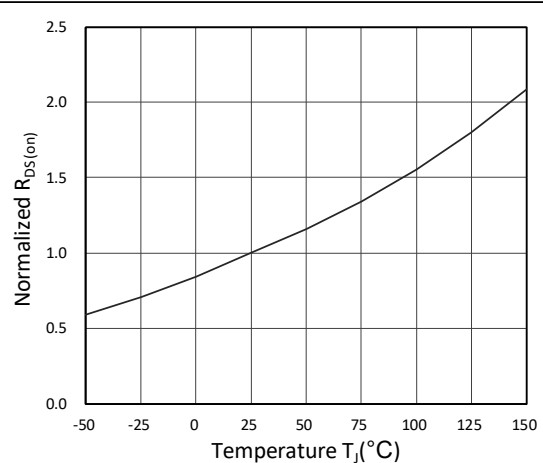


Figure 3. Forward Characteristics of Reverse

Figure 4. $R_{DS(on)}$ vs. V_{GS} Figure 5. $R_{DS(on)}$ vs. I_D Figure 6. Normalized $R_{DS(on)}$ vs. Temperature

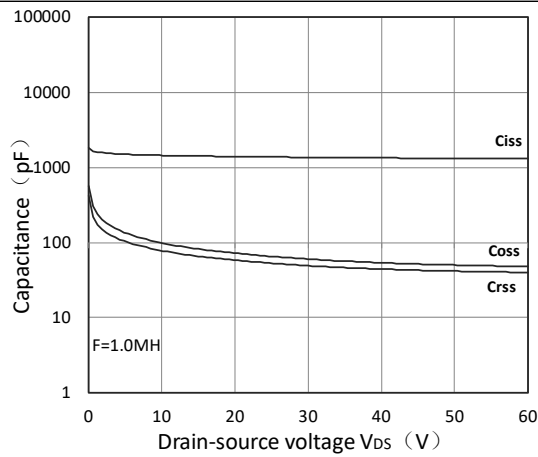


Figure 7. Capacitance Characteristics

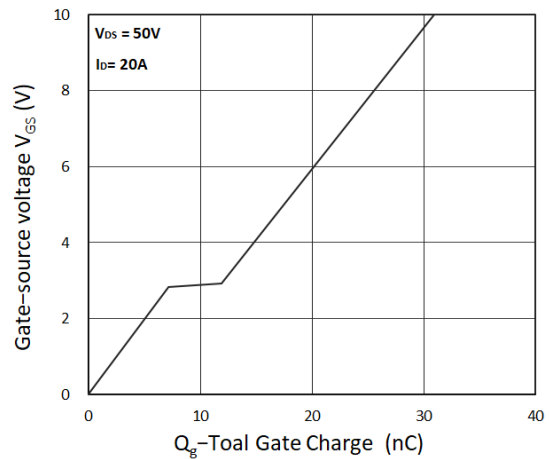


Figure 8. Gate Charge Characteristics

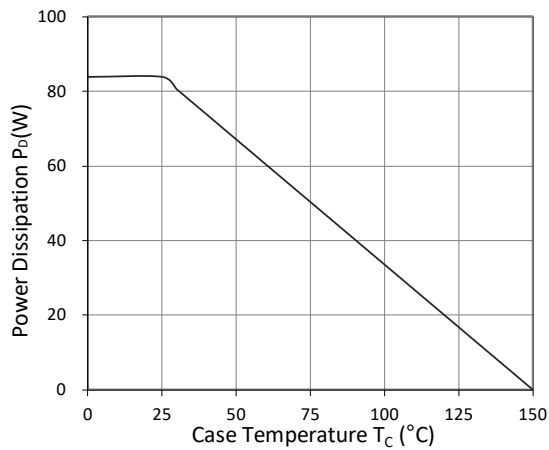


Figure 9. Power Dissipation

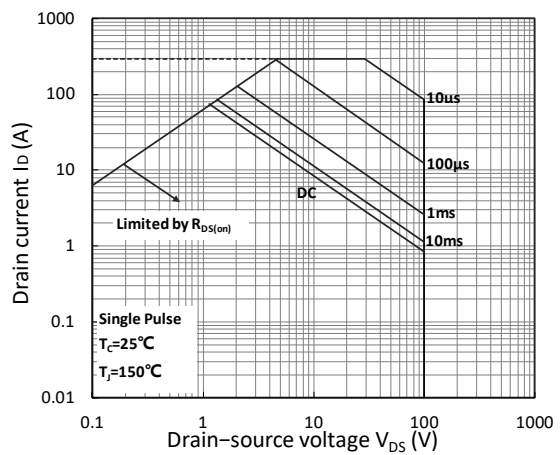


Figure 10. Safe Operating Area

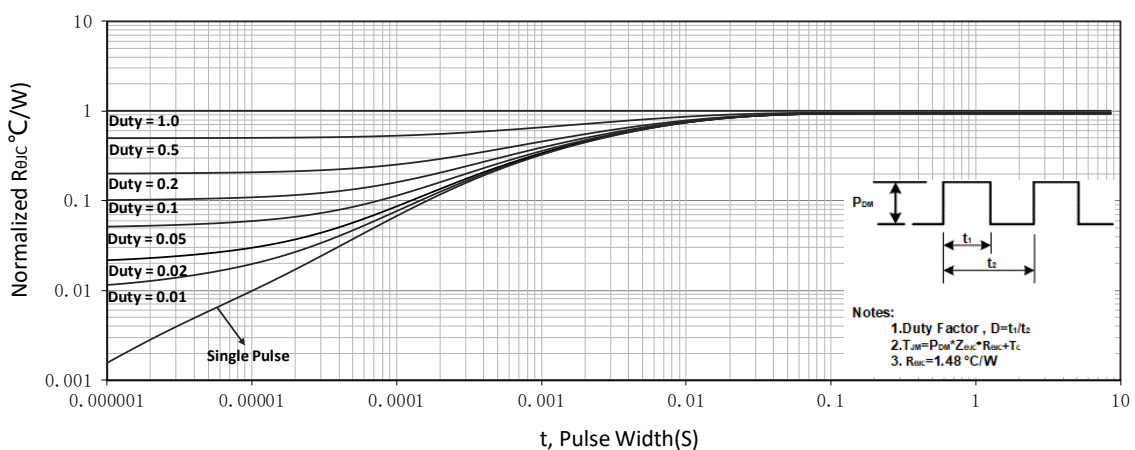


Figure 11. Normalized Maximum Transient Thermal Impedance

Test Circuit

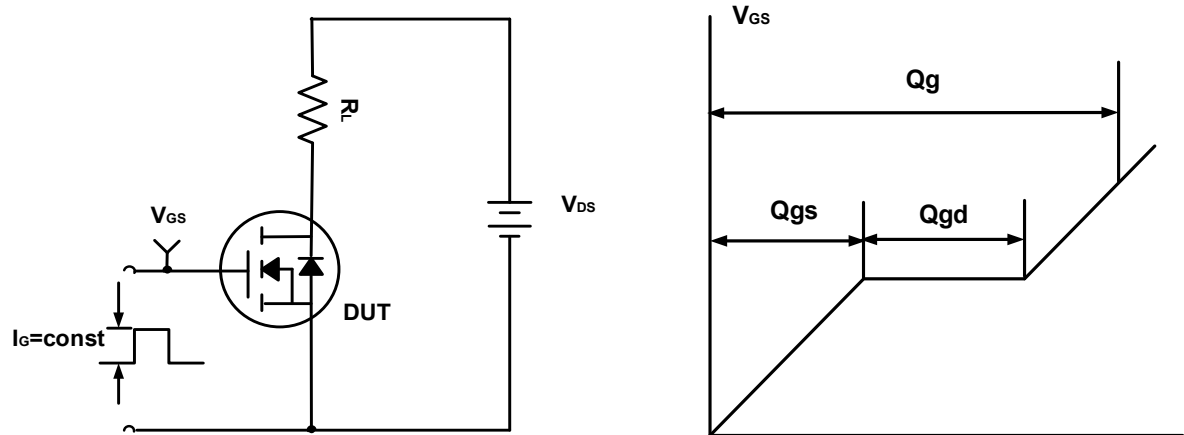


Figure A. Gate Charge Test Circuit & Waveforms

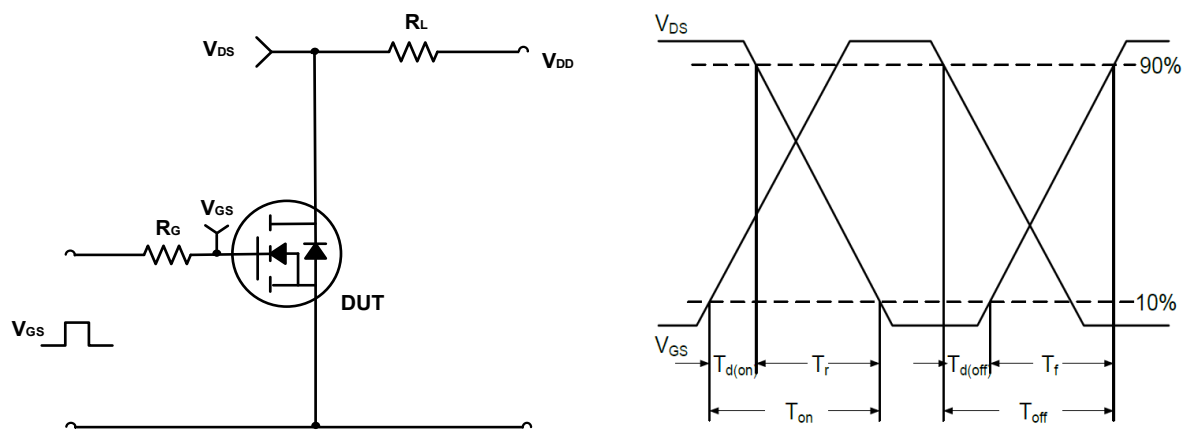


Figure B. Switching Test Circuit & Waveforms

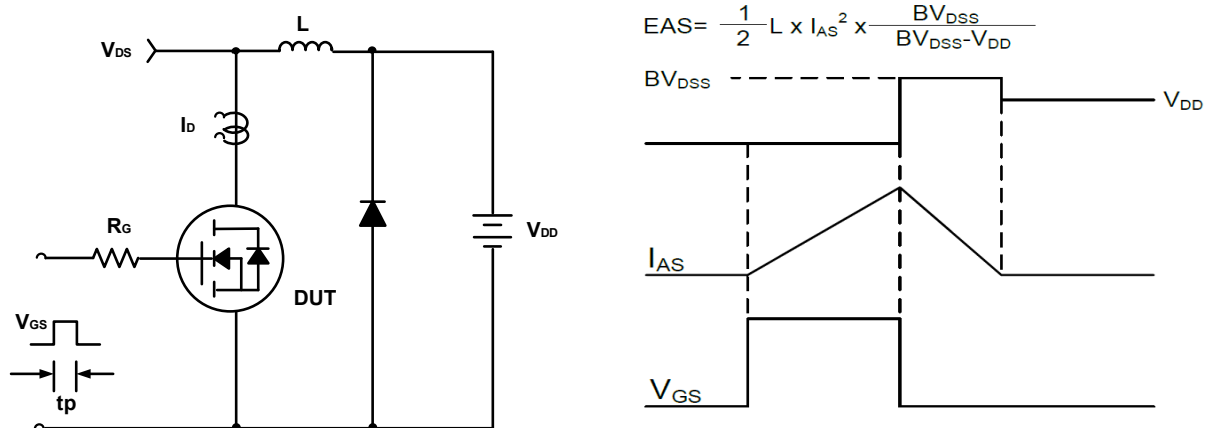
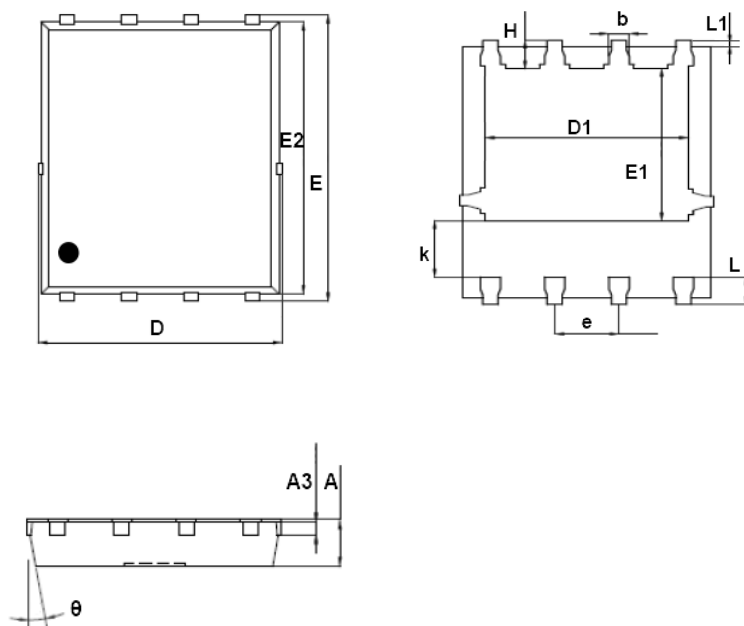


Figure C. Unclamped Inductive Switching Circuit & Waveforms

Mechanical Dimensions for PDFN5060-8L

COMMON DIMENSIONS

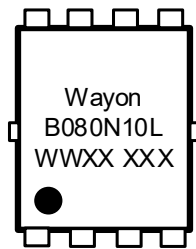


SYMBOL	MM	
	MIN	MAX
A	0.90	1.20
A3	0.15	0.35
D	4.80	5.40
E	5.90	6.35
D1	3.61	4.31
E1	3.30	3.92
E2	5.50	6.06
k	1.10	-
b	0.30	0.51
e	1.27BSC	
L	0.38	0.71
L1	0.05	0.36
H	0.38	0.71
θ	0°	12°

Ordering Information

Part	Package	Marking	Packing method
WMB080N10LG2	PDFN5060-8L	B080N10L	Tape and Reel

Marking Information



B080N10L = Device code

WWXX XXX= Date code

Contact Information

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