

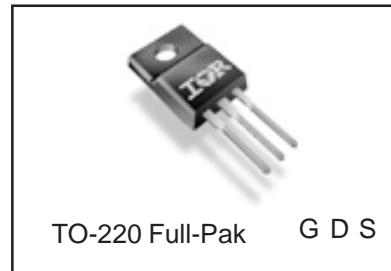
Applications

- Switch Mode Power Supply (SMPS)
- Uninterruptible Power Supply
- High Speed Power Switching
- High Voltage Isolation = 2.5KVRMS[Ⓞ]

V_{DSS}	R_{DS(on)} max	I_D
650V	0.93Ω	5.1A

Benefits

- Low Gate Charge Qg results in Simple Drive Requirement
- Improved Gate, Avalanche and Dynamic dv/dt Ruggedness
- Fully Characterized Capacitance and Avalanche Voltage and Current



Absolute Maximum Ratings

	Parameter	Max.	Units
I _D @ T _C = 25°C	Continuous Drain Current, V _{GS} @ 10V	5.1	A
I _D @ T _C = 100°C	Continuous Drain Current, V _{GS} @ 10V	3.2	
I _{DM}	Pulsed Drain Current [Ⓛ]	21	
P _D @ T _C = 25°C	Power Dissipation	60	W
	Linear Derating Factor	0.48	W/°C
V _{GS}	Gate-to-Source Voltage	± 30	V
dv/dt	Peak Diode Recovery dv/dt [Ⓜ]	2.8	V/ns
T _J	Operating Junction and	-55 to + 150	°C
T _{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds		
	Mounting torque, 6-32 or M3 screw	10 lbf•in (1.1N•m)	

Typical SMPS Topologies

- Single Transistor Flyback
- Single Transistor Forward

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Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	650	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.67	—	V/ $^\circ\text{C}$	Reference to $25^\circ\text{C}, I_D = 1\text{mA}$ ⑥
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.93	Ω	$V_{GS} = 10V, I_D = 3.1\text{A}$ ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
I_{DSS}	Drain-to-Source Leakage Current	—	—	25	μA	$V_{DS} = 650V, V_{GS} = 0V$ $V_{DS} = 520V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
		—	—	250		
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 30V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -30V$

Dynamic @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
g_{fs}	Forward Transconductance	3.9	—	—	S	$V_{DS} = 50V, I_D = 3.1\text{A}$
Q_g	Total Gate Charge	—	—	48	nC	$I_D = 5.2\text{A}$ $V_{DS} = 400V$ $V_{GS} = 10V$, See Fig. 6 and 13 ④
Q_{gs}	Gate-to-Source Charge	—	—	12		
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	19		
$t_{d(on)}$	Turn-On Delay Time	—	14	—	ns	$V_{DD} = 325V$ $I_D = 5.2\text{A}$ $R_G = 9.1\Omega$ $R_D = 62\Omega$, See Fig. 10 ④
t_r	Rise Time	—	20	—		
$t_{d(off)}$	Turn-Off Delay Time	—	34	—		
t_f	Fall Time	—	18	—		
C_{iss}	Input Capacitance	—	1417	—	pF	$V_{GS} = 0V$ $V_{DS} = 25V$ $f = 1.0\text{MHz}$, See Fig. 5
C_{oss}	Output Capacitance	—	177	—		
C_{rss}	Reverse Transfer Capacitance	—	7.0	—		
C_{oss}	Output Capacitance	—	1912	—		
C_{oss}	Output Capacitance	—	48	—		
$C_{oss\ eff.}$	Effective Output Capacitance	—	84	—		

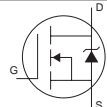
Avalanche Characteristics

	Parameter	Typ.	Max.	Units
E_{AS}	Single Pulse Avalanche Energy②	—	325	mJ
I_{AR}	Avalanche Current①	—	5.2	A
E_{AR}	Repetitive Avalanche Energy①	—	6	mJ

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	2.1	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Junction-to-Ambient	—	65	

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	5.2	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	21		
V_{SD}	Diode Forward Voltage	—	—	1.5	V	$T_J = 25^\circ\text{C}, I_S = 5.2\text{A}, V_{GS} = 0V$ ④
t_{rr}	Reverse Recovery Time	—	493	739	ns	$T_J = 25^\circ\text{C}, I_F = 5.2\text{A}$
Q_{rr}	Reverse Recovery Charge	—	2.1	3.2	μC	$di/dt = 100\text{A}/\mu\text{s}$ ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S + L_D$)				

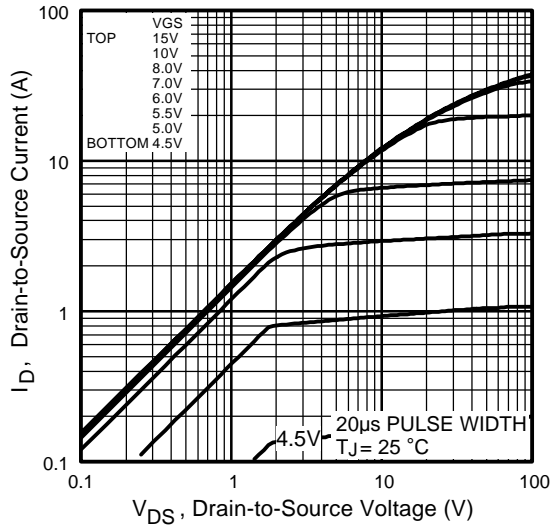


Fig 1. Typical Output Characteristics

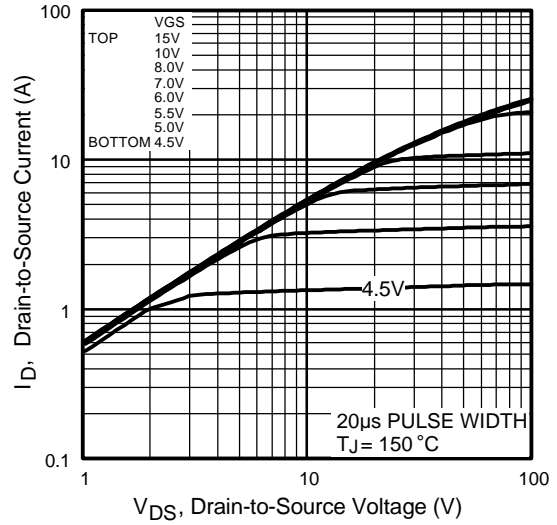


Fig 2. Typical Output Characteristics

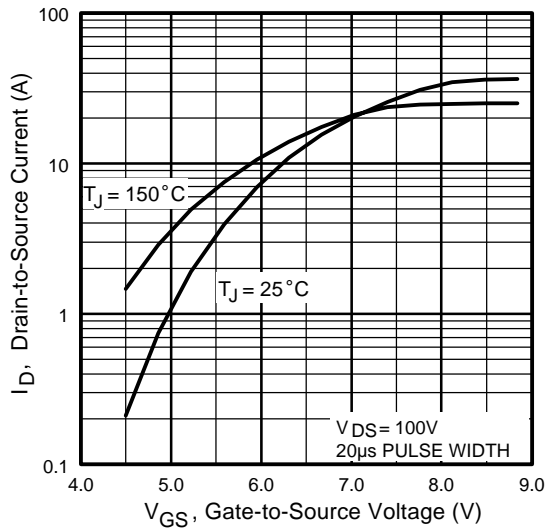


Fig 3. Typical Transfer Characteristics

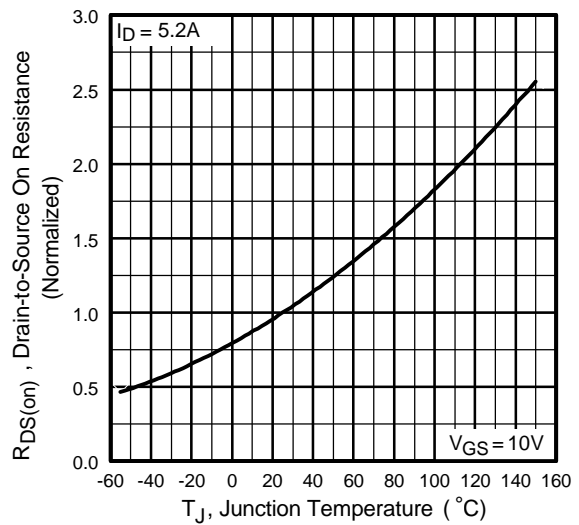


Fig 4. Normalized On-Resistance Vs. Temperature

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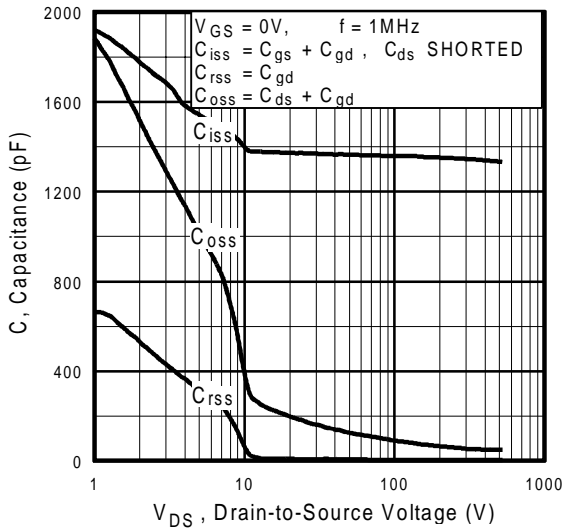


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

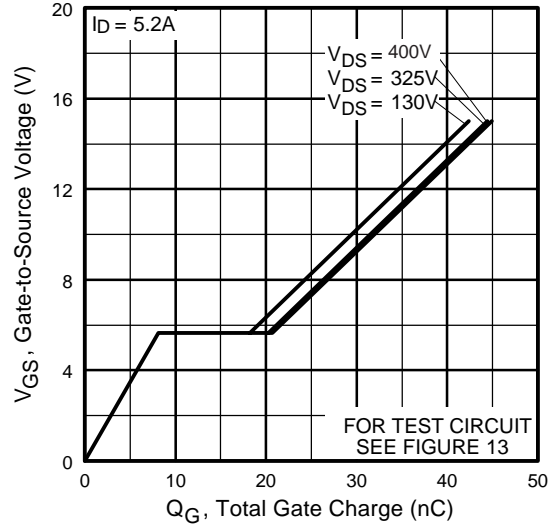


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

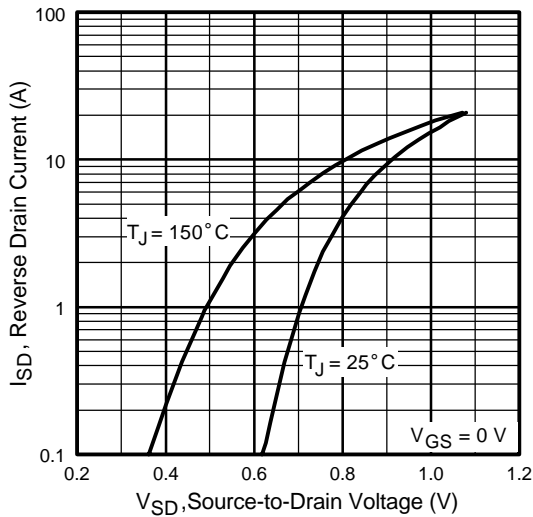


Fig 7. Typical Source-Drain Diode Forward Voltage

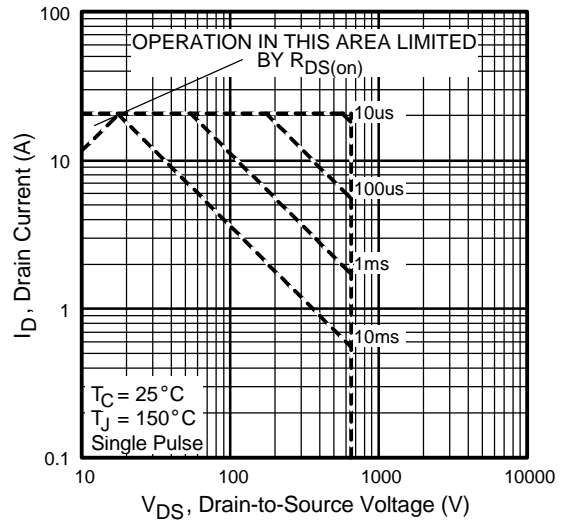


Fig 8. Maximum Safe Operating Area

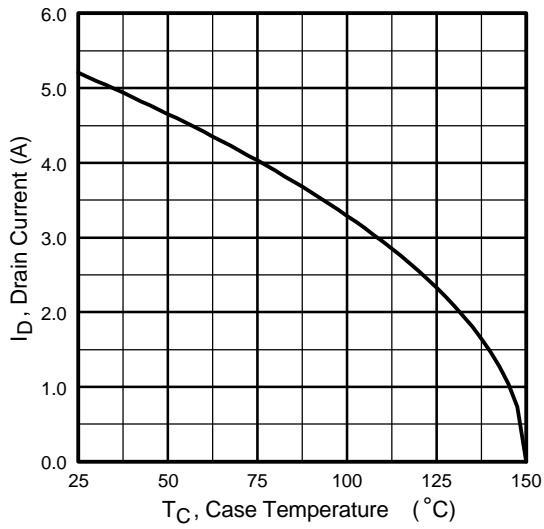


Fig 9. Maximum Drain Current Vs. Case Temperature



Fig 10a. Switching Time Test Circuit



Fig 10b. Switching Time Waveforms

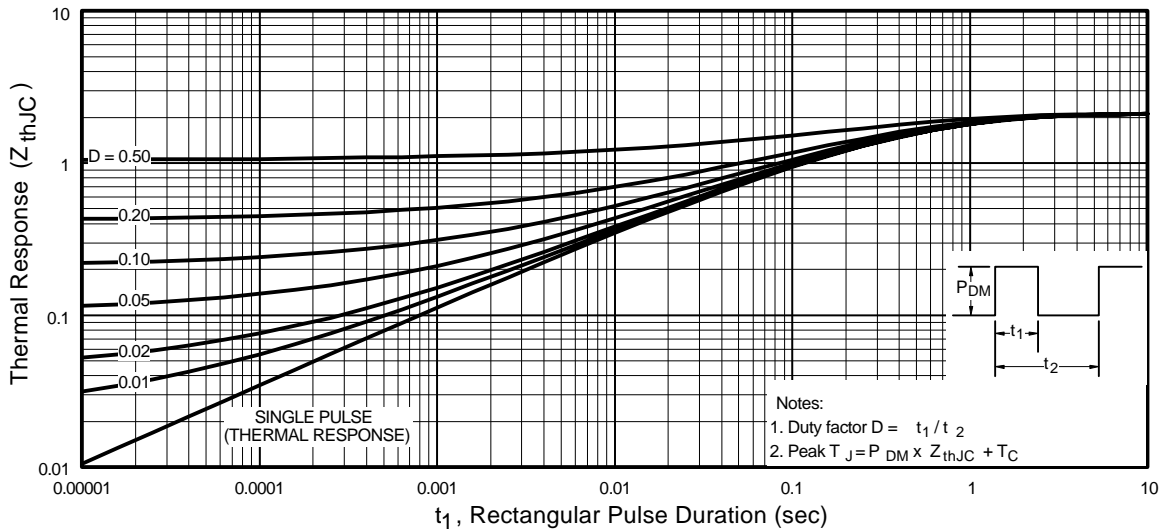


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

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Fig 12a. Unclamped Inductive Test Circuit

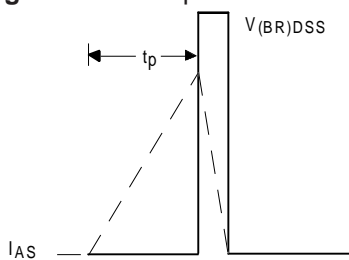


Fig 12b. Unclamped Inductive Waveforms



Fig 13a. Basic Gate Charge Waveform



Fig 13b. Gate Charge Test Circuit

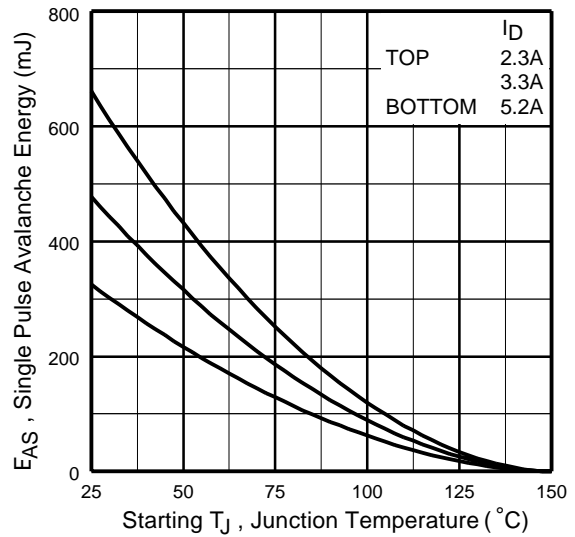


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

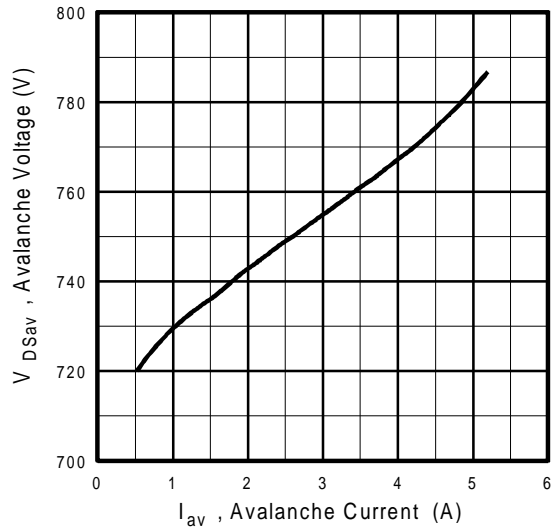


Fig 12d. Typical Drain-to-Source Voltage Vs. Avalanche Current

Peak Diode Recovery dv/dt Test Circuit



* $V_{GS} = 5V$ for Logic Level Devices

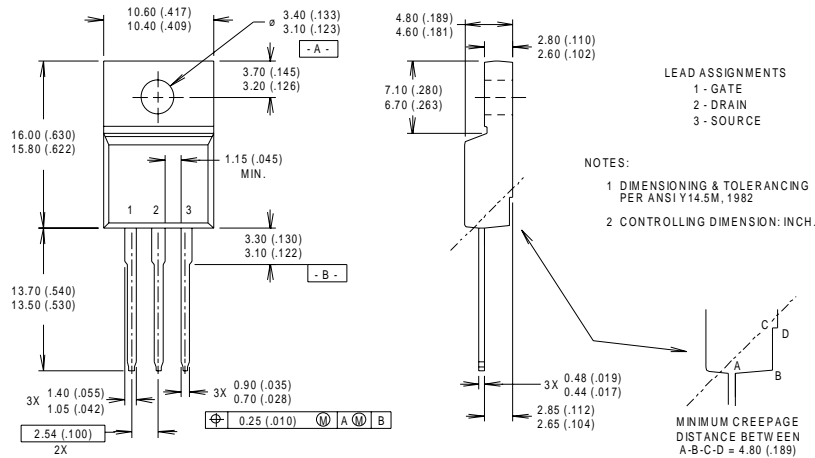
Fig 14. For N-Channel HEXFET® Power MOSFETs

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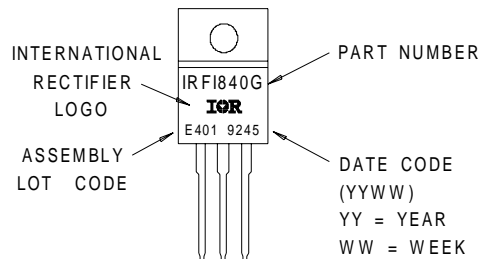
TO-220 Full-Pak Package Outline

Dimensions are shown in millimeters (inches)



TO-220 Full-Pak Part Marking Information

EXAMPLE : THIS IS AN IRF1840G
WITH ASSEMBLY
LOT CODE E401



Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)
- ② Starting $T_J = 25^\circ\text{C}$, $L = 24\text{mH}$
 $R_G = 25\Omega$, $I_{AS} = 5.2\text{A}$. (See Figure 12)
- ③ $I_{SD} \leq 5.2\text{A}$, $di/dt \leq 90\text{A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$,
 $T_J \leq 150^\circ\text{C}$
- ④ Pulse width $\leq 300\mu\text{s}$; duty cycle $\leq 2\%$.
- ⑤ C_{OSS} eff. is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 80% V_{DSS}
- ⑥ $t = 60\text{s}$, $f = 60\text{Hz}$

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Data and specifications subject to change without notice. 6/00