NOVOSENSE
纳芯微电子

NSiP83086

Signal Isolated RS-485 Transceiver With Integrated DC to DC Converter

Datasheet (EN) 1.0

Product Overview

NSiP83086 series are high reliability isolated full duplex RS-485 transceiver with integrated DC to DC converter. The NSiP83086 isolated DC to DC converter uses on-chip transformer. The feedback PWM signal is sent to primary side(Isolator Side1) by a digital isolator based on Novosense capacity isolation technology. The NSiP83086 series are safety certified by UL1577 supporting 5kVrms insulation withstand voltage, while the high integrated solution can help to simplify system design and improve reliability.

The Bus pins of NSiP83086 are protected from ±8kV system level ESD to GND_2. The device features a fail-safe circuitry, which guarantees a logic-high receiver output when the receiver inputs are open or shorted. The device have 96k Ω input impedance that allows up to 256 transceivers on the bus.

Key Features

- Up to 5000Vrms Insulation voltage
- ISO-Power integrated isolated DC-to-DC converter
- I/O voltage range supports 1.8~5.5V MCU
- Power supply voltage:
  - VDD: 4.5V to 5.5V for NSiP83086
  - 3V to 5.5V for NSiP83086C and NSiP83086V
  - VDDL: 1.8V to 5.5V
- Over current and over temperature protection
- High CMTI: ±150kV/us
- Data rate: 16Mbps
- Up to 256 transceivers on the bus
- High system level EMC performance:
  - BUS Pins meet IEC61000-4-2 ±8kV ESD
  - Other Pins meet IEC61000-4-2 ±7kV ESD
- Operation temperature: -40℃~105℃
- RoHS-compliant packages: SOW20 SOW16

Safety Regulatory Approvals

- UL recognition: up to 5000V_{RMS} for 1 minute per UL1577
- CQC certification per GB4943.1-2022
- CSA component notice 5A
- DIN VDE V 0884-11:2017-01

Applications

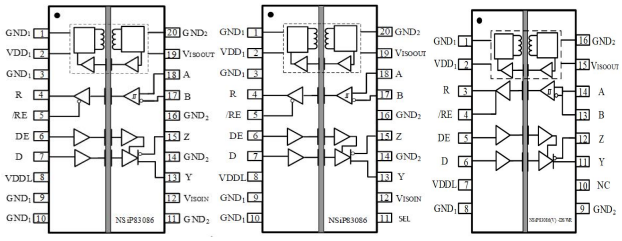
- Industrial automation system
- Isolated RS-485 communication
- Smart electric meter and water meter
- Security and protection monitoring

Device Information

Part Number	*Package*	*Body Size*
NSiP83086(C)(V)-DSWTR	SOW20	12.80mm × 7.50mm
NSiP83086(V)-DSWR	SOW16	10.30mm x 7.50mm

Note: (C), (V) could be empty representing 5V output version. V represents 3.3V output version, C version has SEL pin which can choose 3.3/5V output

Functional Block Diagrams



NSiP83086(V)-DSWTR NSiP83086C-DSWTR NSiP83086(V)-DSWR

Figure 1. NSiP83086 Block Diagrams

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1. Pin Configuration and Functions

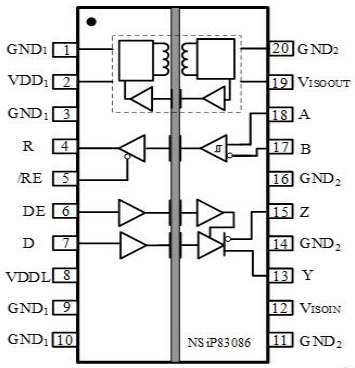


Figure 1.1 NSiP83086(V)-DSWTR Package

Table1.1 NSiP83086(V)-DSWTR Pin Configuration and Description

PIN NO.	SYMBOL	FUNCTION
1	GND_1	Ground 1, the ground reference for Isolator Side 1
2	VDD_1	Power Supply for Isolator Side 1 ,It is recommended this pin have a 0.1μF + 10 μF capacitor to GND_1 (Pin1,Pin3)
3	GND_1	Ground 1, the ground reference for Isolator Side 1
4	R	Receiver output
5	/RE	Receiver enable input, this is an active low input
6	DE	Driver enable input, this is an active high input
7	D	Driver transmit data input
8	VDDL	I/O Power Supply input, Side1 I/O logic level
9	GND_1	Ground 1, the ground reference for Isolator Side 1
10	GND_1	Ground 1, the ground reference for Isolator Side 1
11	GND_2	Ground 2, the ground reference for Isolator Side 2
12	V_{ISOIN}	Isolated power supply input. This pin must be connected externally to V_{ISOOUT}. It is recommended this pin have a 0.1 μF capacitor to GND_2 (Pin11). Connect this pin to V_{ISOOUT} through a ferrite bead and short trace length for operation.
13	Y	Non-inverting Driver Output. When the driver is disabled, or when VDDL is powered down, Pin Y is put into a high impedance state to avoid overloading the bus.
14	GND_2	Ground 2, the ground reference for Isolator Side 2
15	Z	Inverting Driver Output. When the driver is disabled, or when VDD is powered down, Pin Z is put into a high impedance state to avoid overloading the bus.
16	GND_2	Ground 2, the ground reference for Isolator Side 2
17	B	Inverting Receiver Input

18	A	Non-inverting Receiver Input
19	V_{ISOOUT}	Isolated Power Supply Output. This pin must be connected externally to V_{ISOIN}. It is recommended this pin have a 0.1 μF and 10μF capacitor to GND_2 (Pin20). Connect this pin through a ferrite bead and short trace length to V_{ISOIN} for operation.
20	GND_2	Ground 2, the ground reference for Isolator Side 2

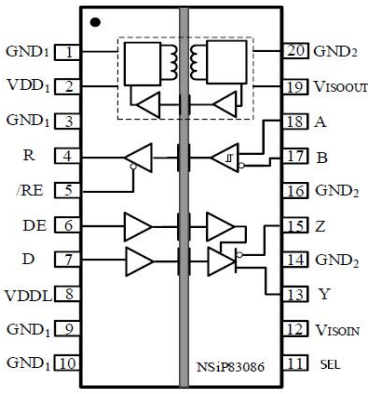


Figure 1.2 NSiP83086C-DSWTR Package

Table1.2NSiP83086C-DSWTR Pin Configuration and Description

PIN NO.	*SYMBOL*	*FUNCTION*
1	GND_1	Ground 1, the ground reference for Isolator Side 1
2	VDD_1	Power Supply for Isolator Side 1 ,It is recommended this pin have a 0.1μF + 10 μF capacitor to GND_1 (Pin1,Pin3)
3	GND_1	Ground 1, the ground reference for Isolator Side 1
4	R	Receiver output
5	/RE	Receiver enable input, this is an active low input
6	DE	Driver enable input, this is an active high input
7	D	Driver transmit data input
8	VDDL	I/O Power Supply input, Side1 I/O logic level
9	GND_1	Ground 1, the ground reference for Isolator Side 1
10	GND_1	Ground 1, the ground reference for Isolator Side 1
11	SEL	VISO output voltage select, V_{ISOOUT} =5V when SEL is floating or connect to V_{ISOIN}, V_{ISOOUT} =3.3V when SEL short to GND_2
12	V_{ISOIN}	Isolated power supply input. This pin must be connected externally to V_{ISOOUT}. It is recommended this pin have a 0.1 μF capacitor to GND_2 . Connect this pin to V_{ISOOUT} through a ferrite bead and short trace length for operation.
13	Y	Non-inverting Driver Output. When the driver is disabled, or when VDDL is powered down, Pin Y is put into a high impedance state to avoid overloading the bus.
14	GND_2	Ground 2, the ground reference for Isolator Side 2

15	Z	Inverting Driver Output. When the driver is disabled, or when VDD is powered down, Pin Z is put into a high impedance state to avoid overloading the bus.
16	GND_2	Ground 2, the ground reference for Isolator Side 2
17	B	Inverting Receiver Input
18	A	Non-inverting Receiver Input
19	V_{ISOOUT}	Isolated Power Supply Output. This pin must be connected externally to V_{ISOIN}. It is recommended this pin have a 0.1 μF and 10μF capacitor to GND_2 (Pin20). Connect this pin through a ferrite bead and short trace length to V_{ISOIN} for operation.
20	GND_2	Ground 2, the ground reference for Isolator Side 2

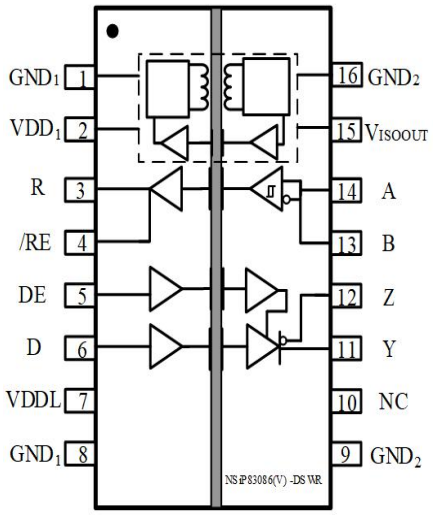


Figure 1.3 NSiP83086(V)-DSWR Package

Table1.3NSiP83086(V)-DSWR Pin Configuration and Description

PIN NO.	SYMBOL	FUNCTION
1	GND_1	Ground 1, the ground reference for Isolator Side 1
2	VDD_1	Power Supply for Isolator Side 1. It is recommended this pin have a 0.1 μF + 10 μF capacitor to GND_1 (Pin1)
3	R	Receiver output
4	/RE	Receiver enable input, this is an active low input
5	DE	Driver enable input, this is an active high input
6	D	Driver transmit data input
7	VDDL	I/O Power Supply input, Side1 I/O logic level
8	GND_1	Ground 1, the ground reference for Isolator Side 1
9	GND_2	Ground 2, the ground reference for Isolator Side 2
10	NC	Not Connected

11	Y	Non-inverting Driver Output. When the driver is disabled, or when VDD is powered down, Pin Y is put into a high impedance state to avoid overloading the bus.
12	Z	Inverting Driver Output. When the driver is disabled, or when VDD is powered down, Pin Z is put into a high impedance state to avoid overloading the bus.
13	B	Inverting Receiver Input
14	A	Non-inverting Receiver Input
15	V_{ISOOUT}	Isolated Power Supply Output. It is recommended this pin have a 0.1 μF and 10μF capacitor to GND_2 (Pin16).
16	GND_2	Ground 2, the ground reference for Isolator Side 2.

2. Absolute Maximum Ratings

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Power Supply Voltage	VDD,VDDL	-0.5		6	V	
Maximum Input Voltage	/RE, DE, D	-0.4		VDDL+0.4	V	
Driver Output/Receiver Input Voltage	V_A, V_B, V_Y, V_Z	-7		12	V	
R output current	I_O	-15		15	mA	
Operating Temperature	Topr	-40		105	℃	
Storage Temperature	Tstg	-40		150	℃	
Electrostatic discharge	HBM			±8000	V	
	CDM			±2000	V	

3. Recommended Operating Conditions

Parameters	Symbol	Min	Typ	Max	Unit
NSiP83086 Power Supply Voltage	VDD	4.5	5	5.5	V
NSiP83086C and NSiP83086V Power Supply Voltage	VDD	3	3.3/5	5.5	V
Operating Temperature	Topr	-40		105	℃
Side1 High Level Input Voltage	V_{IH}	0.7*VDDL		VDDL	V
Side1 Low Level Input Voltage	V_{IL}	0		0.3*VDDL	V
Data rate	DR			16	Mbps

4. Thermal Information

Parameters	Symbol	SOW20	SOW16	Unit
IC Junction-to-Air Thermal Resistance	θ_{JA}	68.5	61	°C/W
Junction-to-top characterization parameter	ψ_{JT}	17.1	10.2	°C/W
Junction-to-board characterization parameter	ψ_{JB}	50.9	37.2	°C/W

5. Specifications

5.1. DC Electrical Characteristics

(VDD=4.5V~5.5V, VDDL=1.8~5.5V, Ta=-40℃ to 105℃. Unless otherwise noted, Typical values are at VDD=VDDL=5V,V_{ISOOUT}=5V, Ta = 25℃)

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Comments*
Power supply voltage NSiP83086	VDD_1	4.5		5.5	V	
	VDDL	1.8		5.5	V	
Power supply voltage NSiP83086C/NSiP83086V	VDD_1	3		5.5	V	
	VDDL	1.8		5.5	V	
Supply current condition: VDD=4.5V~5.5V, VDDL=1.8~5.5V, Ta=-40℃ to 105℃.						
Supply current V_{ISOOUT} = 5V	IDD (500kbps)		72	90	mA	VDD=5V VDDL=3.3V R_L=120 Ω
			118	140	mA	VDD=5V VDDL=3.3V R_L=54 Ω
	IDD (16Mbps)		100	130	mA	VDD=5V VDDL=3.3V R_L=120 Ω
			130	160	mA	VDD=5V VDDL=3.3V R_L=54 Ω
	IDDL			5	mA	
Supply current condition: VDD=3~5.5V, VDDL=1.8~5.5V, Ta=-40℃ to 105℃.						
Supply current V_{ISOOUT} = 3.3V	IDD (500kbps)		40	55	mA	VDD=5V VDDL=3.3V R_L=120 Ω
			61	80	mA	VDD=5V VDDL=3.3V R_L=54 Ω
	IDD (16Mbps)		45	65	mA	VDD=5V VDDL=3.3V R_L=120 Ω
			60	80	mA	VDD=5V VDDL=3.3V R_L=54 Ω
	IDDL			5	mA	
Isolated supply voltage	V_{ISOOUT}		5		V	NSiP83086
	V_{ISOOUT}		3.3/5		V	NSiP83086C
	V_{ISOOUT}		3.3		V	NSiP83086V
Thermal-Shutdown Threshold	T_{TS}		165		℃	
Thermal-Shutdown Hysteresis	T_{TSH}		15		℃	
Common Mode Transient Immunity	CMTI	100	150		kV/us	Figure 5.12
Side1						
Input High Voltage	V_{IH}	0.7*VDDL			V	DE, D, /RE
Input Low Voltage	V_{IL}			0.3*VDDL	V	DE, D, /RE
Input Current	I_I	-20		20	uA	D, DE, /RE

Output Voltage High	V_{OH}	0.8*VDDL			V	IOH = -4mA
Output Voltage Low	V_{OL}			0.2*VDDL	V	IOL = 4mA
Output Short-Circuit Current	I_{OSR}			150	mA	$0 \le V_R \le$VDDL
Three-State Output Current	I_{OZR}			15	uA	$0 \le V_R \le$ VDDL , /RE = high
Input Capacitance	C_{IN}		2		pF	DE, D, /RE
Driver						
Differential Output Voltage	$\lvert V_{OD} \rvert$			5.5	V	No Load， V_{ISOOUT}=5V
		2.7		5.5	V	Figure 5.7,R_L=120Ω V_{Isoout}=5V
		2.1		5.5	V	Figure 5.7,R_L=54Ω (RS-485) V_{Isoout}=5V
Change in magnitude of the differential output voltage	$\Delta\lvert V_{OD} \rvert$			0.2	V	, R_L=120Ω or R_L=54Ω V_{Isoout}=5V
Common-Mode Output Voltage	$\lvert V_{OC} \rvert$			3	V	, R_L=120Ω or R_L =54Ω V_{Isoout}=5V
Change in Magnitude of Common-Mode Voltage	$\Delta\lvert V_{OC} \rvert$			0.2	V	, R_L=120Ω or R_L =54Ω V_{Isoout}=5V
Driver Short-Circuit Output Current	I_{OSD}			200	mA	$0 \le V_{Test} \le$ 12 V
		-200			mA	$-7V \le V_{Test} \le 0V$
Output Leakage Current (Y and Z) Full-Duplex	I_O			200	uA	DE=0V, V_{Test}=12V
		-200			uA	DE=0V, V_{Test}=-7V
Receiver						
Input Current (A and B)	I_A , I_B			200	uA	DE=0V, V_{ISOIN}=0V, V_{Test}=12V
		-200			uA	DE=0V, V_{ISOIN}=0V, V_{Test}=-7V
Receiver Differential Threshold Voltage	V_{TH}	-200	-125	-10	mV	V_{CM}=0V
Receiver Input Hysteresis	ΔV_{TH}		15		mV	V_A+V_B=0
Receiver Input Resistance	R_{IN}	96			kΩ	$-7V \le V_{CM} \le$ 12V, DE=0V

5.2. Switching Electrical Characteristics

(VDD=3V~5.5V,VDDL=1.8~5.5V, Ta=-40℃ to 105℃. Unless otherwise noted, Typical values are at VDD=VDDL = 5V, Ta = 25℃)

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Comments*
Driver						
Maximum Data Rate	f_{MAX}			16	Mbps	
Driver Propagation Delay	t_{PLH}		22	60	ns	See Figure 5.8, R_L=54Ω, C_L=50pF
	t_{PHL}		21	60	ns	See Figure 5.8, R_L=54Ω, C_L=50pF
Driver Pulse Width Distortion, $\|t_{PHL} - t_{PLH}\|$	t_{skew}		1	8	ns	See Figure 5.8, R_L=54Ω, C_L=50pF
Driver Output Falling Time or Rising time	t_F			15	ns	See Figure 5.8, R_L=54Ω, C_L=50pF
	t_R			15	ns	See Figure 5.8, R_L=54Ω, C_L=50pF
Driver Enable to Output High	t_{ZH}		22.8	50	ns	See Figure 5.9, R_L=120Ω, C_L=50pF
Driver Enable to Output Low	t_{ZL}		19.1	50	ns	See Figure 5.9, R_L=120Ω, C_L=50pF
Driver Disable to Output High	t_{HZ}		28	50	ns	See Figure 5.9, R_L=120Ω, C_L=50pF
Driver Disable to Output Low	t_{LZ}		27.1	50	ns	See Figure 5.9, R_L=120Ω, C_L=50pF
Receiver						
Maximum Data Rate	f_{MAX}	16			Mbps	
Receiver Propagation Delay	t_{PLH}		65.8	140	ns	See Figure 5.10, C_L=15pF
	t_{PHL}		71.4	140	ns	See Figure 5.10, C_L=15pF
Receiver Pulse Width Distortion, $\|t_{PHL} - t_{PLH}\|$	t_{skew}		5.6	12	ns	See Figure 5.10, C_L=15pF
Receiver Output Falling Time or Rising time	t_F			15	ns	See Figure 5.10, C_L=15pF
	t_R			15	ns	See Figure 5.10, C_L=15pF
Receiver Enable to Output High	t_{ZH}		6	15	ns	See Figure 5.11, R_L=1kΩ, C_L=15pF
Receiver Enable to Output Low	t_{ZL}		6	15	ns	See Figure 5.11, R_L=1kΩ, C_L=15pF
Receiver Disable to Output High	t_{HZ}		8	15	ns	See Figure 5.11,

						R_L=1kΩ, C_L=15pF
Receiver Disable to Output Low	t_{LZ}		8	15	ns	See Figure 5.11, R_L=1kΩ, C_L=15pF

5.3. Typical Performance Characteristics

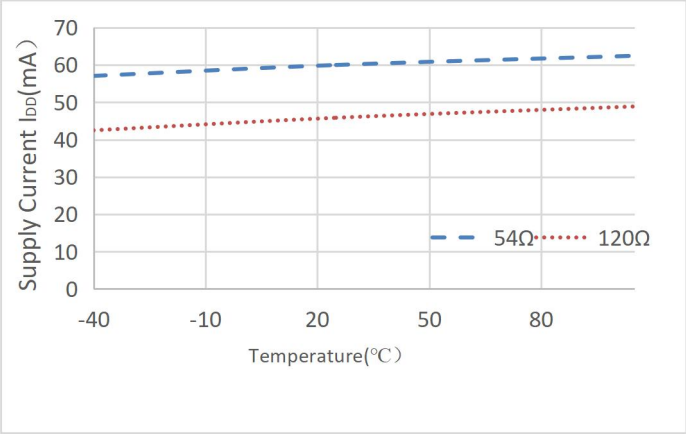


Figure 5.1 NSiP83086 supply current vs Temperature
(Data Rate=16MHz,DE=VDDL,/RE=GND,VDD=5V,V_{ISOOUT}=3.3V)

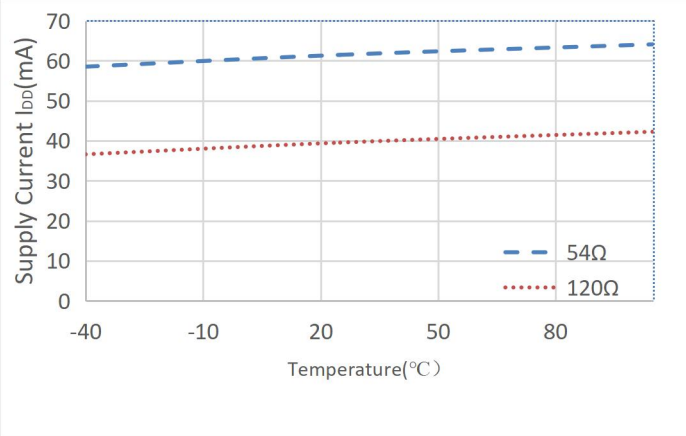


Figure 5.2 NSiP83086 supply current vs Temperature
(Data Rate=500KHz,DE=VDDL,/RE=GND,VDD=5,V_{ISOOUT}=3.3V)

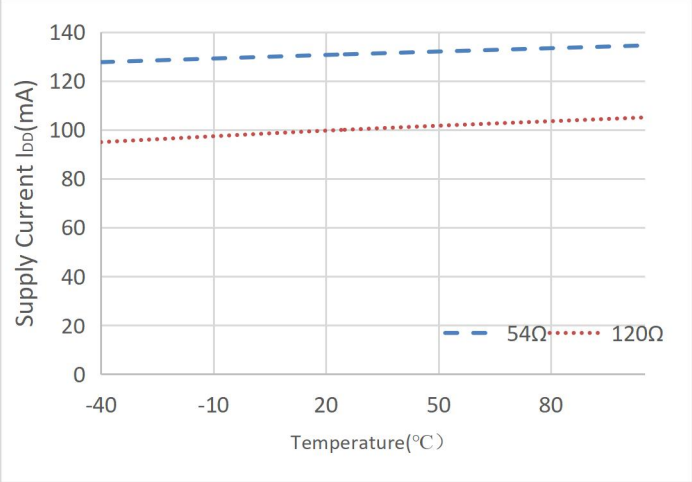


Figure 5.3 NSiP83086 supply current vs Temperature
(Data Rate=16MHz,DE=VDDL,/RE=GND,VDD=5V,V_{ISOOUT}=5V)

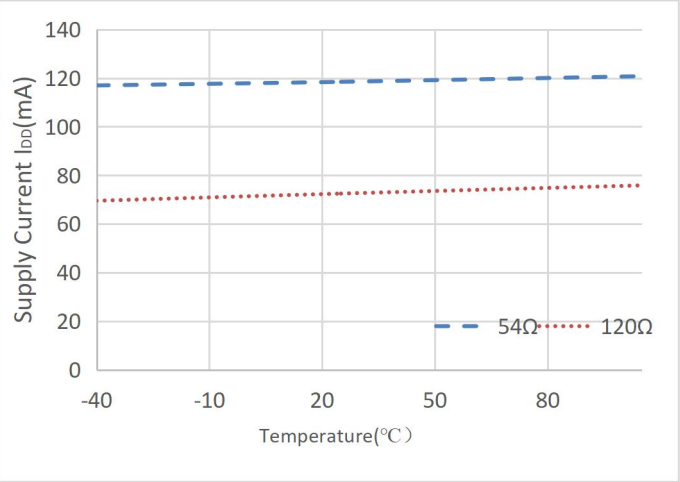


Figure 5.4 NSiP83086 supply current vs Temperature
(Data Rate=500KHz,DE=VDDL,/RE=GND,VDD=5V,V_{ISOOUT}=5V)

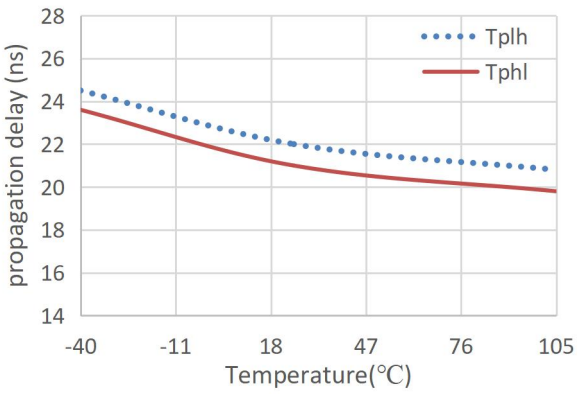


Figure 5.5 Driver Propagation Delay vs Temperature

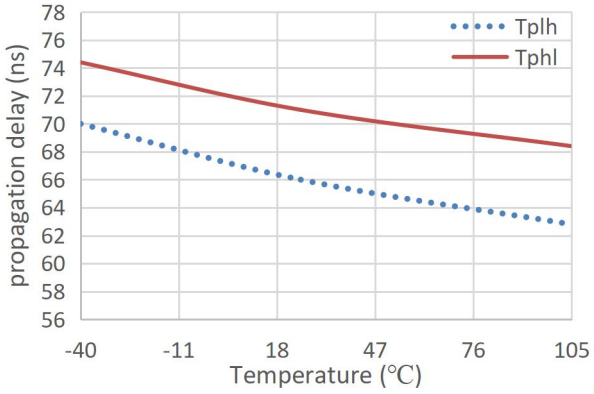


Figure 5.6 Receiver Propagation Delay vs Temperature

5.4. Parameter Measurement Information

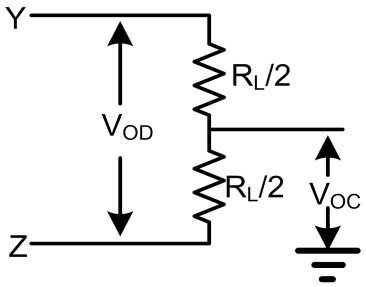


Figure 5.7 Driver DC Test Load

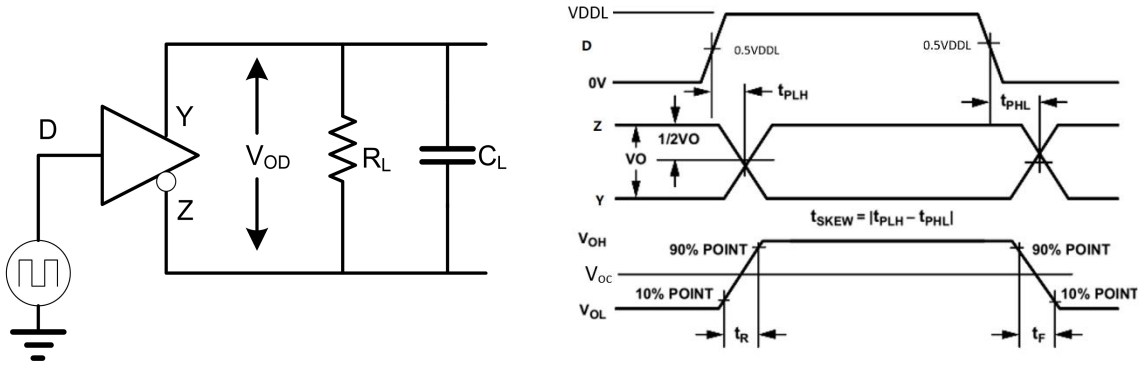
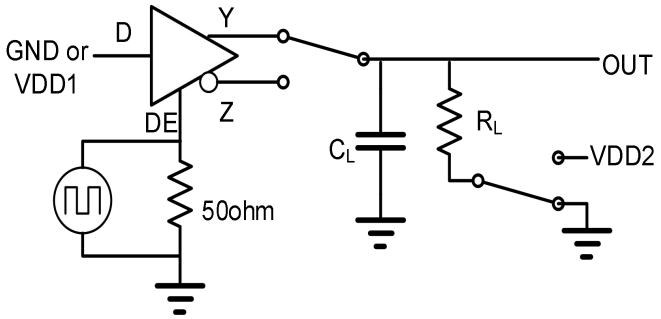


Figure5.8 Driver Timing Test Circuit and waveform



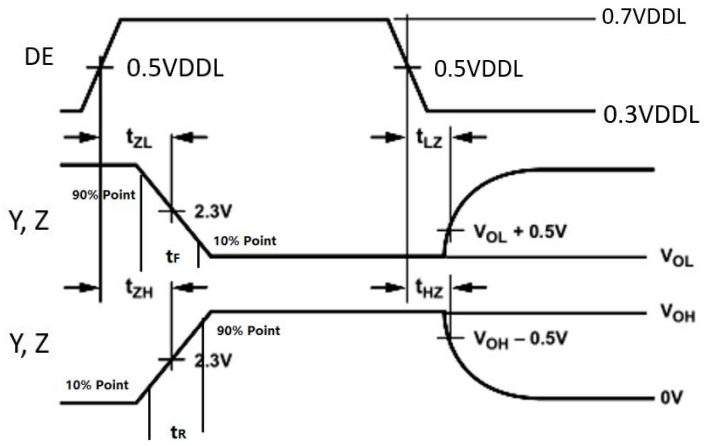


Figure5.9 Driver Enable Disable Timing Test Circuit and waveform

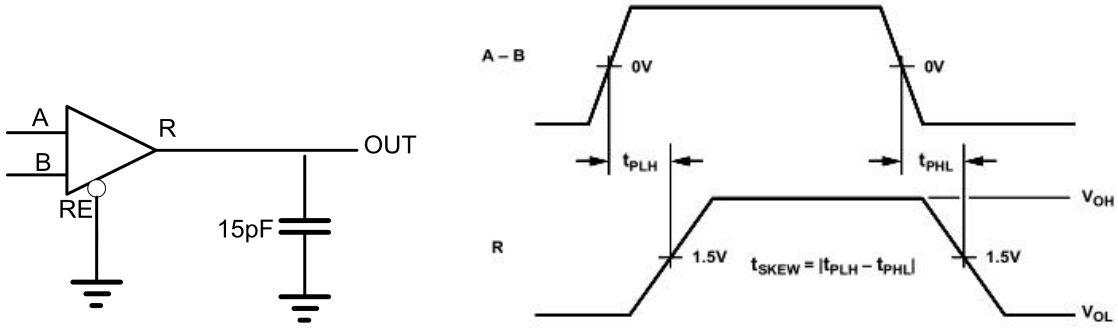


Figure 5.10 Receiver Propagation Delay Test Circuit and waveform

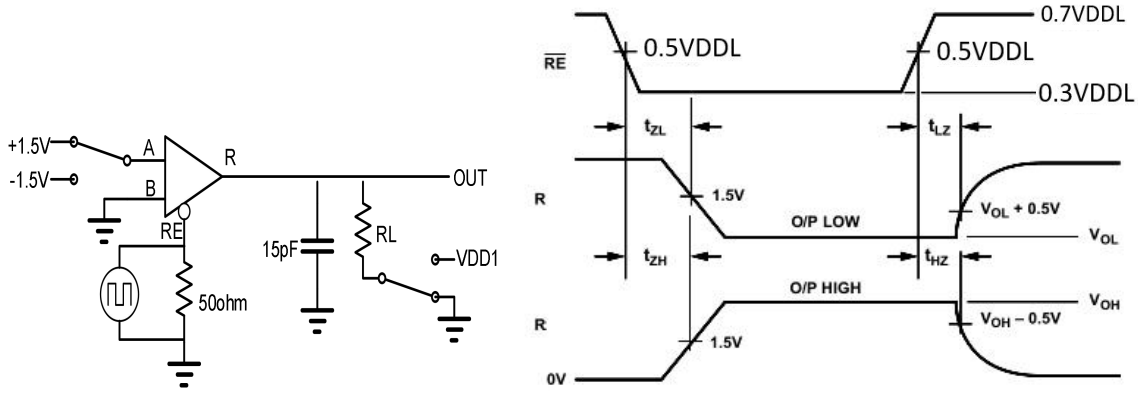


Figure 5.11 Receiver Enable Disable Timing Test Circuit and waveform

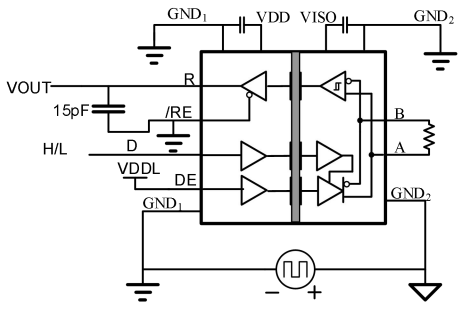


Figure5.12 Common-Mode Transient Immunity Test Circuit

6. High Voltage Feature Description

6.1. Insulation and Safety Related Specifications

Parameters	*Symbol*	*Value*	*Unit*	*Comments*
Minimum External Air Gap (Clearance)	CLR	8.0	mm	Shortest terminal-to-terminal distance through air
Minimum External Tracking (Creepage)	CPG	8.0	mm	Shortest terminal-to-terminal distance across the package surface
Distance through the insulation	DTI	16	um	Minimum internal gap (internal clearance – capacitive signal isolation)
		100	um	Minimum internal gap (internal clearance – transformer power isolation)
Tracking Resistance (Comparative Tracking Index)	CTI	>600	V	DIN EN 60112 (VDE 0303-11); IEC 60112
Material Group		I		

6.2. DIN VDE V 0884-11（VDE V 0884-11）:2017-01 INSULATION CHARATERISTICS

Description	*Test Condition*	*Symbol*	*Value*	*Unit*
Installation Classification per DIN VDE 0110				
For Rated Mains Voltage ≤ 150Vrms			Ⅰ to Ⅳ	
For Rated Mains Voltage ≤ 300Vrms			Ⅰ to Ⅳ	
For Rated Mains Voltage ≤ 600Vrms			Ⅰ to Ⅲ	
Climatic Classification			40/105/21	
Pollution Degree per DIN VDE 0110, Table 1			2	
Maximum repetitive peak isolation voltage	AC voltage(bipolar)	V_{IORM}	1166	Vpeak
Maximum working isolation voltage	AC voltage(TDDB) test	V_{IOWM}	824	Vrms
	DC Voltage	V_{IOWM}	1166	V_{DC}
Input to Output Test Voltage, Method B1	$V_{IORM} \times 1.5 = V_{pd(m)}$, 100%production test, $t_{ini} = t_m = 1$ sec, partial discharge < 5 pC	$V_{pd(m)}$	1749	Vpeak
Input to Output Test Voltage, Method A				
After Environmental Tests Subgroup 1	$V_{IORM} \times 1.2 = V_{pd(m)}$, $t_{ini} = 60$ sec, $t_m = 10$ sec, partial	$V_{pd(m)}$	1399	Vpeak

	discharge < 5 pC			
After Input and /or Safety Test Subgroup 2 and Subgroup 3	$V_{IORM} \times 1.2 = V_{pd(m)}$, t_{ini} = 60 sec, t_m = 10 sec, partial discharge < 5 pC	$V_{pd(m)}$	1399	Vpeak
Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$; t = 60 s (qualification); $V_{TEST} = 1.2 \times V_{IOTM}$; t = 1 s (100% production)	V_{IOTM}	7000	Vpeak
Maximum Surge Isolation Voltage	Test method per IEC60065,1.2/50us waveform, $V_{TEST} = 1.3xV_{ISOM}$	V_{IOSM}	5384	Vpeak
Isolation resistance	V_{IO} =500V	R_{IO}	>10^{12}	Ω
Isolation capacitance	f = 1MHz	C_{IO}	0.6	pF
Total Power Dissipation at 25℃ for SOW20 Package		P_S	1459	mW
Safety input, output, or supply current for SOW20 Package	θ_{JA} = 68.5°C/W, V_I = 5.5 V, T_J = 125 °C, T_A = 25 °C	Is	265	mA
Total Power Dissipation at 25℃ for SOW16 Package		P_S	1639	mW
Safety input, output, or supply current for SOW16 Package	θ_{JA} = 61°C/W, V_I = 5.5 V, T_J = 125 °C, T_A = 25 °C	I_S	298	mA
Safety Temperature		Ts	125	℃

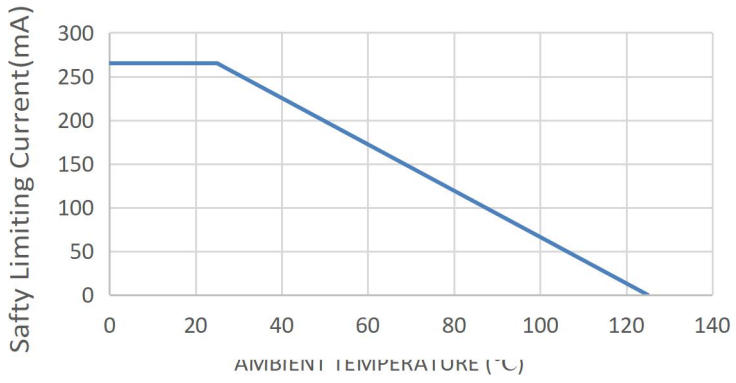


Figure 6.1NSiP83086 Thermal Derating Curve for SOW20 package, Dependence of Safety Limiting Values with Case Temperature per DIN VDE V 0884-11

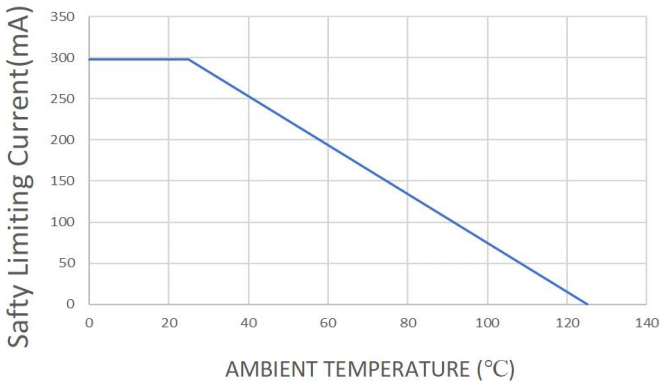


Figure 6.2NSiP83086 Thermal Derating Curve for SOW16 package, Dependence of Safety Limiting Values with Case Temperature per DIN VDE V 0884-11

6.3. Regulatory Information

The NSiP83086 are approved or pending approval by the organizations listed in table.

CUL		*VDE*	*CQC*
UL 1577 Component Recognition Program[1]	Approved under CSA Component Acceptance Notice 5A	DIN VDE V 0884-11(VDE V 0884-11):2017-01[2]	Certified by CQC11-471543-2012 GB4943.1-2022
Single Protection, 5000V_{RMS} Isolation voltage	Single Protection, 5000V_{RMS}Isolation voltage	Basic Insulation 1166Vpeak, V_{IOSM}=5384V_{PEAK}	Basic insulation
File (pending)	File (pending)	File (pending)	File (pending)

7. Function Description

NSiP83086 is a high reliability isolated full duplex RS-485 transceiver. Data isolation is achieved using Novosense integrated capacitive isolation that allows data transmission between the logic side and the Bus side. The 83086 series are safety certified by UL1577 supporting 5kV_{RMS} insulation withstand voltage.

7.1. True Fail-Safe Receiver Inputs

The devices feature fail-safe circuitry, which guarantees a logic-high receiver output when the receiver inputs are open or shorted. The receiver threshold is fixed between -10mV and -200mV, which meets EIA/TIA-485 standard. If the differential input voltage (V_A-V_B) is greater than or equal to -10mV, receiver output R is logic high. In the case of a terminated bus with all transmitters disabled, the differential input voltage is pulled to zero by the termination resistors. Due to the receiver threshold, the receiver output R is logic high.

7.2. Truth Tables

Table 7.1 Driver Function Table

VDD_1 status	*Input (D)*	*Enable Input (DE)*	*Outputs Y*	*Z*
PU	H	H	H	L
PU	L	H	L	H
PU	X	L	Z	Z
PU	X	OPEN	Z	Z
PU	OPEN	H	H	L
PD	X	X	Z	Z

Table 7.2 Receiver Function Table[1]

VDD status	*Differential Input (VA-VB)*	*Enable Input (/RE)*	*Output (R)*
PU	≥-10mV	L/Open	H
PU	≤-200mV	L/Open	L
PU	Open/Short	L/Open	H
PU	X	H	Z
PU	Idle	L	H
PD	X	X	Z

[1] PD= Powered down; PU= Powered up; H= Logic High; L= Logic Low; X= Irrelevant; Z= High Impedance;

7.3. EMI Considerations

NSIP83086 use a small on-chip transformer to provide power for RS485 Transceiver. The on-chip transformer operates at high frequency, which may degrade EMI performance, to achieve better EMI performance, special considerations must be taken during PCB layout. Please see the application note if needed.

7.4. Output Short and Over Temperature Protection

The NSiP83086 series are protected against output short for V_{ISOOUT}. When short on V_{ISOOUT} occurs, the device will be in Hiccup mode and the power transferred will be limit, which will limit the temperature of the device to protect the device.

The NSiP83086 series also protected against over temperature. When the chip is over 165℃, it will be shut down until the temperature of below 145℃.

8. Application Note

8.1. 256 Transceivers on the Bus

The devices have a 1/8-unit-load receiver input impedance (96kΩ) that allows up to 256 transceivers on the bus. Connect any combination of these devices, and/or other RS-485 devices, for a maximum of 32 unit-loads to the line.

8.2. ESD Protection

ESD protection structures are enhanced on all pins to protect against electrostatic discharge encountered during handing and assembly. The Bus pins have extra protection against static electricity to bus side (V_{ISOOUT} side).

ESD protection can be tested in various ways. Below is the ESD spec of the devices.

Bus pins:

- ±8kV using the Contact Discharge method specified in IEC 61000-4-2

Other pins except bus pins:

- ±7kV using the Contact Discharge method specified in IEC 61000-4-2

8.3. Layout Considerations

The NSiP83086 requires a 10μF+0.1μF bypass capacitor between VDD_1 and GND_1, 10uF+0.1uF bypass capacitor between V_{ISOOUT} and GND_2. The capacitor should be placed as close as possible to the package. To eliminate line reflections, each cable end (A-B, Y-Z) is terminated with a resistor, whose value matches the characteristic impedance of the cable(54Ω/120Ω). It's good practice to place the bus connectors and termination resistor as close as possible to the A and B, Y and Z pins.

8.4. Typical Application

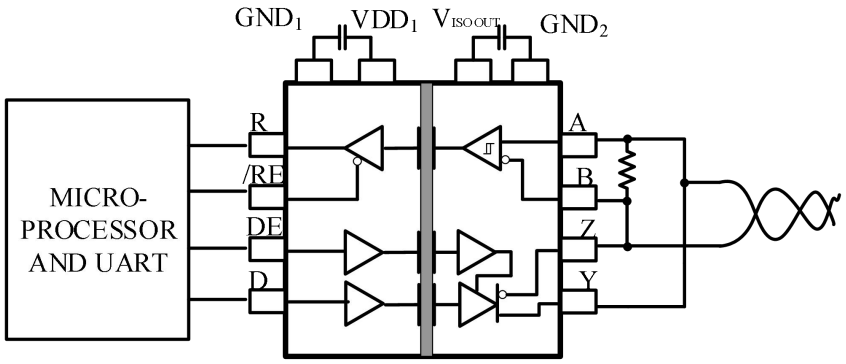


Figure 8.1 NSiP83086 in Half-Duplex RS-485 Mode

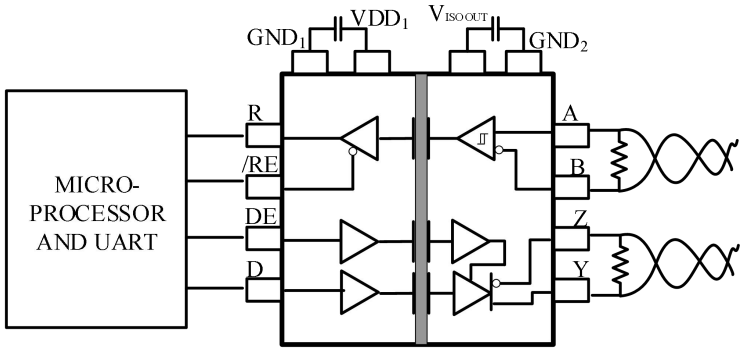


Figure 8.2 NSiP83086 typical application circuit

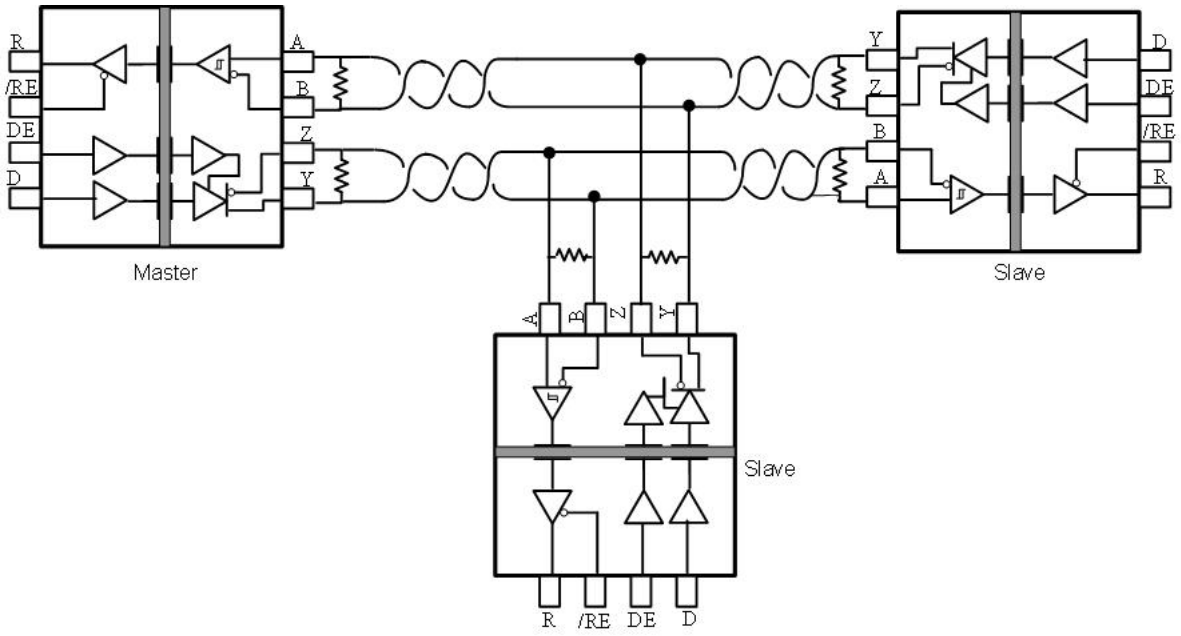
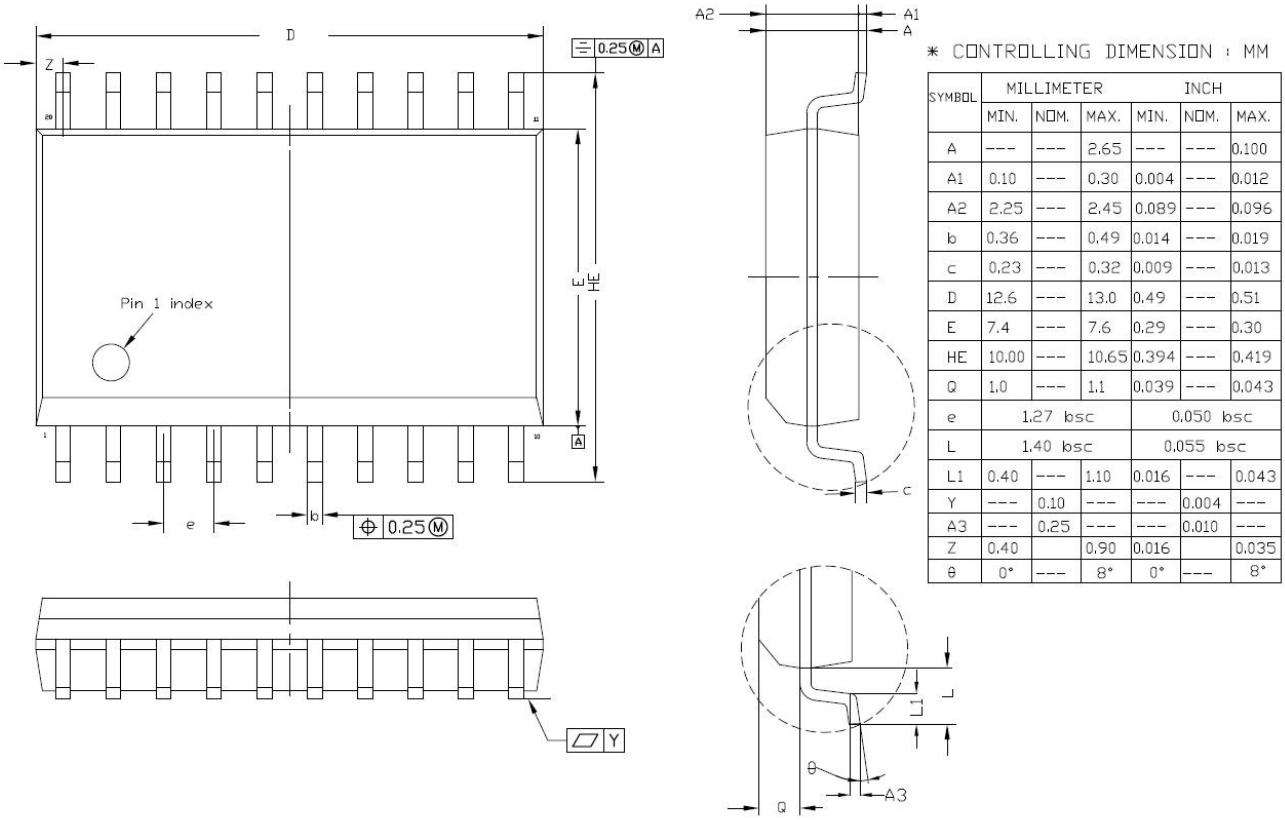


Figure 8.3 Typical isolated Full-Duplex RS-485 application

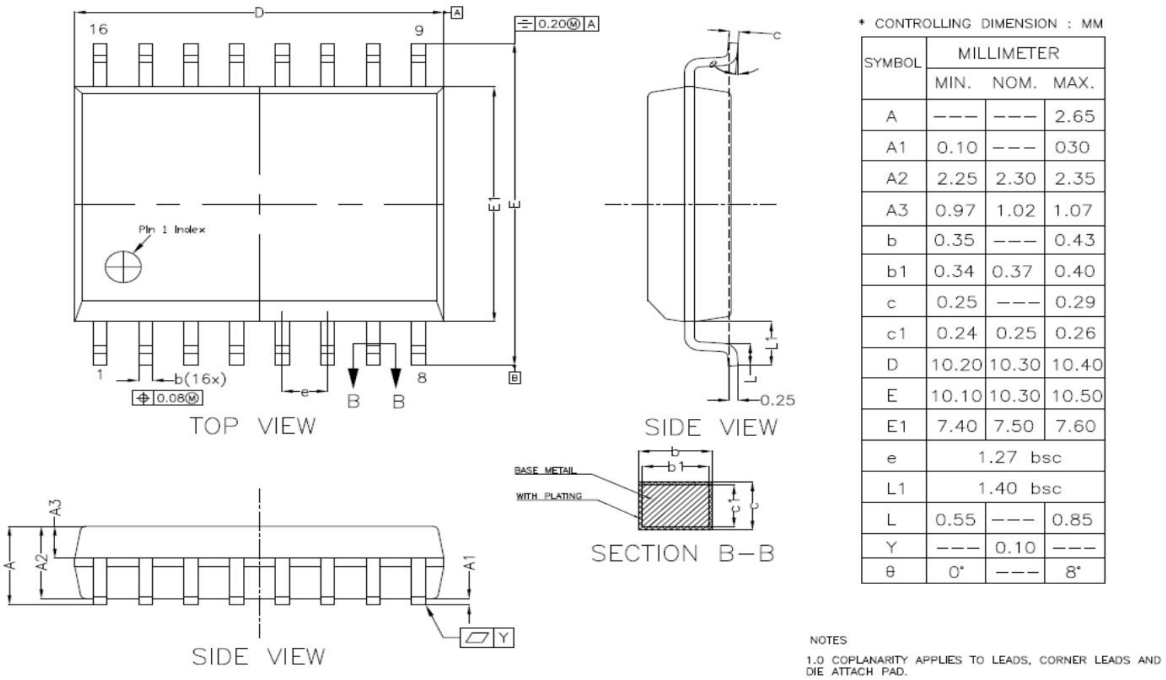
9. Package Information



* CONTROLLING DIMENSION : MM

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	---	---	2.65	---	---	0.100
A1	0.10	---	0.30	0.004	---	0.012
A2	2.25	---	2.45	0.089	---	0.096
b	0.36	---	0.49	0.014	---	0.019
c	0.23	---	0.32	0.009	---	0.013
D	12.6	---	13.0	0.49	---	0.51
E	7.4	---	7.6	0.29	---	0.30
HE	10.00	---	10.65	0.394	---	0.419
Q	1.0	---	1.1	0.039	---	0.043
e	1.27 bsc			0.050 bsc		
L	1.40 bsc			0.055 bsc		
L1	0.40	---	1.10	0.016	---	0.043
Y	---	0.10	---	---	0.004	---
A3	---	0.25	---	---	0.010	---
Z	0.40		0.90	0.016		0.035
θ	0°	---	8°	0°	---	8°

Figure 9.1 SOW20 Package Shape and Dimension in millimeters and inches



* CONTROLLING DIMENSION : MM

SYMBOL	MILLIMETER		
	MIN.	NOM.	MAX.
A	---	---	2.65
A1	0.10	---	030
A2	2.25	2.30	2.35
A3	0.97	1.02	1.07
b	0.35	---	0.43
b1	0.34	0.37	0.40
c	0.25	---	0.29
c1	0.24	0.25	0.26
D	10.20	10.30	10.40
E	10.10	10.30	10.50
E1	7.40	7.50	7.60
e	1.27 bsc		
L1	1.40 bsc		
L	0.55	---	0.85
Y	---	0.10	---
θ	0°	---	8°

NOTES

1.0 COPLANARITY APPLIES TO LEADS, CORNER LEADS AND DIE ATTACH PAD.

Figure 9.2 SOW16 Package Shape and Dimension in millimeters

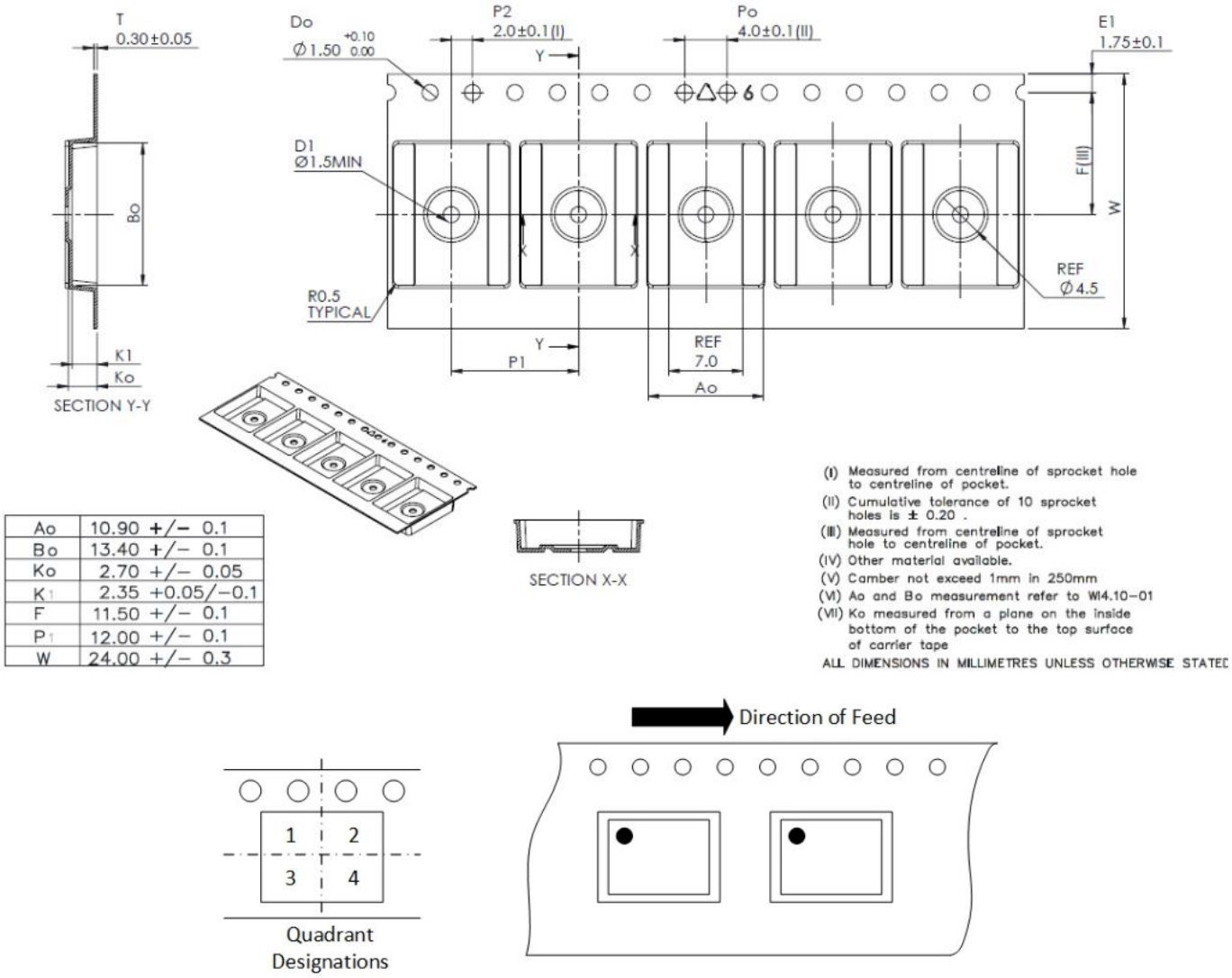
10. Ordering Information

Part Number	Isolation Rating (kV_{RMS})	V_{ISOOUT}	Duplex	Max Data Rate (Mbps)	MSL	Temperature	No. of Nodes	Package Type	Package Drawing	SPQ
NSiP83086-DSWTR	5	5V	Full	16	3	-40 to 105°C	256	SOP20(300mil)	SOW20	1000
NSiP83086C-DSWTR	5	5/3.3V	Full	16	3	-40 to 105°C	256	SOP20(300mil)	SOW20	1000
NSiP83086V-DSWTR	5	3.3V	Full	16	3	-40 to 105°C	256	SOP20(300mil)	SOW20	1000
NSiP83086-DSWR	5	5V	Full	16	3	-40 to 105°C	256	SOP16(300mil)	SOW16	1000
NSiP83086V-DSWR	5	3.3V	Full	16	3	-40 to 105°C	256	SOP16(300mil)	SOW16	1000
	NOTE: All packages are RoHS-compliant with peak reflow temperatures of 260 °C according to the JEDEC industry standard classifications and peak solder temperatures.									

11. Documentation Support

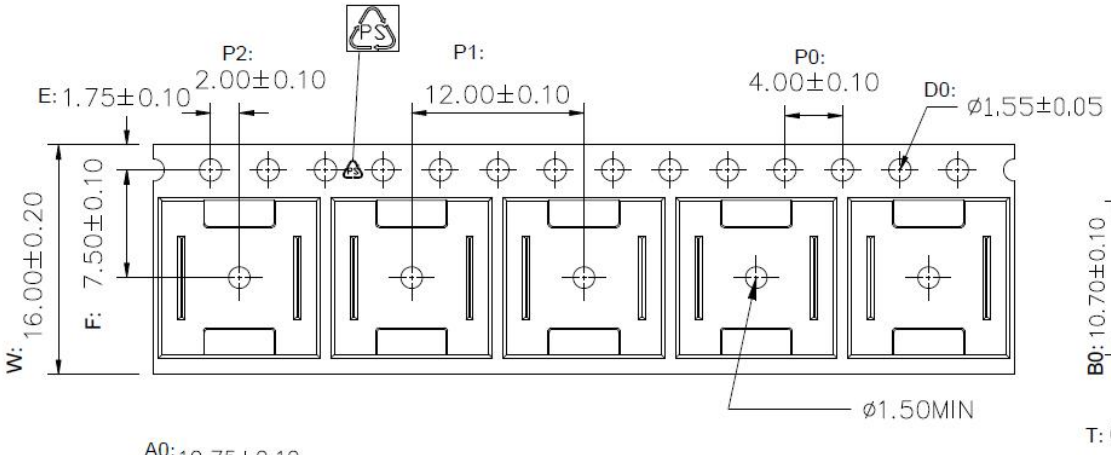
Part Number	Product Folder	Datasheet	Application Note
NSiP83086	tbd	tbd	tbd

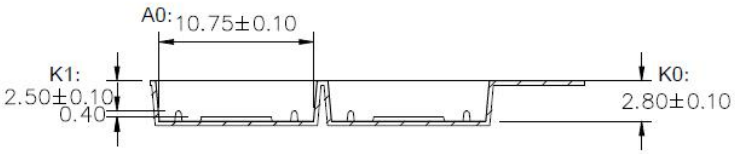
12. Tape And Reel Information



Ao	10.90 +/− 0.1
Bo	13.40 +/− 0.1
Ko	2.70 +/− 0.05
K1	2.35 +0.05/−0.1
F	11.50 +/− 0.1
P1	12.00 +/− 0.1
W	24.00 +/− 0.3

Figure 12.1 Tape and Reel Information of SOW20





1. 10 sprocket hole pitch cumulative tolerance ±0.20 .
2. Carrier camber is within 1 mm in 250 mm.
3. Material : Black Conductive Polystyrene Alloy .
4. All dimensions meet EIA-481 requirements.
5. Thickness : 0.30±0.05mm.
6. Packing length per 22" reel : 378 Meters.(復卷 N=122）
7. Component load per 13" reel : 1000 pcs.
8. Surface resistivity :10^{5} ~ 10^{10}Ω/□

RoHS

W	16.00±0.20
A0	10.75±0.10
B0	10.70±0.10
K0	2.80±0.10
K1	2.50±0.10

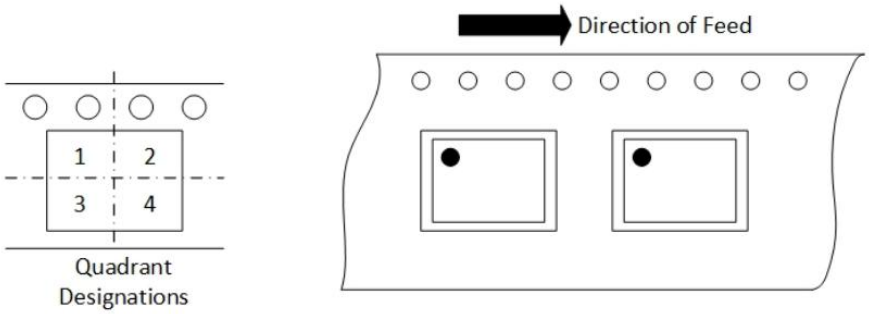


Figure 12.2 Tape and Reel Information of SOW16

13. Revision History

Revision	Description	Date
1.0	Initial Version	2022/11/30

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